REMARKS

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

Claims 1-20 are pending in the present application. Claims 1, 10 and 17 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The Abstract of the disclosure is objected to for reasons stated in the Office Action. The Abstract is amended in a manner that is believed to overcome the objection. Entry of the amendments to the Abstract and removal of the objection are respectfully requested.

Applicant notes with appreciation that the Office Action indicates at page 5, second paragraph that claims 2-9, 11 and 13-19 are objected to, but would be allowable if rewritten in independent form. The Applicant will defer submission of the rewritten allowable claims, pending consideration of the present Amendment.

Claims 1, 10, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han (United States Patent No. 6,175,387) in view of Suen, *et al.* (United States Patent No. 6,552,750). In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Reconsideration of the rejections is respectfully requested.

The Applicant's invention according to amended independent claim 1 is directed to an image processing apparatus for displaying a plurality of input data ansynchronously input through different channels on one display device and converting frame rates of the input data in accordance with an output frame rate of the display device (see, for example, Figure 1 of the present specification). Input buffers 100, 105 buffer input data IN1, IN2 which are externally and asynchronously input through at least two channels by different input clock signals CK_G, CK_V and output the buffered data as first data GDATA1, VDATA1 and first data enabling signals GEN1, VEN1. Data synchronizing units 110, 115 synchronize the first data output from

the input buffer unit with an output clock signal CK_0 in response to the input clock signals CK_G, CK_V and the first data enabling signals GEN1, VEN1 and output synchronized data as second data GDATA2, VDATA2 and second data enabling signals GEN2, VEN2 in response to each of the first data enabling signals GEN1, VEN1. A first memory 120 multiplexes the second data according to time sharing, stores the second data in different regions, and outputs the stored second data FDATA1 in response to a first memory enabling signal FEN1. A second memory 130 writes and reads the data FDATA1 output from the first memory 120 in response to a frame buffer control signal FBCON. A third memory 140 stores data FBDATA output from the second memory 130 and comprises a single output terminal OUT for outputting the stored data FDATA2 as a display signal in response to a second memory enabling signal FEN2. A memory control unit 150 (i) detects underflow conditions in the first memory 120 and detects overflow conditions in the third memory 140, (ii) generates the first memory enabling signal FEN1 that is applied to the first memory 120 to control data flow between the first memory 120 and the second memory 130, (iii) generates the frame buffer control signal FBCON that is applied to the second memory 130 to control frame rates of the input data IN1, IN2 and the display signal in response to the underflow and overflow conditions, and (iv) generates the second memory enabling signal FEN2 that is applied to the third memory 140 to control data flow between the second memory 130 and the third memory 140.

The Applicant's invention according to amended independent claim 10 is directed to an image processing method for displaying a plurality of input data asynchronously input through different channels on one display device and converting frame rates of the input data in accordance with an output frame rate of the display device (see, for example, Figures 5A-5B of the present specification). The plurality of input data is bufferered by using each of input clock signals and synchronizing each of buffered data with an output clock signal. The plurality of input data synchronized with the output clock signal is stored in a first memory in response to each of input enabling signals. A write address of a first memory is compared with a read address of the first memory to determine whether data stored in the first memory are stored in a second memory and to detect underflow conditions in the first memory. Frame rates of each of

the plurality of input data are compared with that of an output display signal to control data write and read of the second memory. A write address of a third memory is compared with a read address of the third memory to determine whether output data of the second memory are stored in the second memory and to detect overflow conditions in the third memory, and data stored in the third memory is output through a single output terminal of the third memory as a display signal for displaying on the display device.

The claims are amended herein to clarify certain details of the present invention. Specifically, independent claim 1 is amended to clarify that a third memory stores data output from a second memory and comprises a single output terminal for outputting the stored data as a display signal in response to a second memory enabling signal. In addition, independent claim 1 is amended to clarify that a memory control unit (i) detects underflow conditions in a first memory and detects overflow conditions in the third memory, (ii) generates a first memory enabling signal that is applied to the first memory to control data flow between the first memory and the second memory, (iii) generates a frame buffer control signal that is applied to the second memory to control frame rates of input data and to control frame rates of the display signal in response to the underflow and overflow conditions, and (iv) generates the second memory enabling signal that is applied to the third memory to control data flow between the second memory and the third memory. Independent claim 10 is amended herein to clarify that a write address of a first memory is compared with a read address of the first memory to determine whether data stored in the first memory are stored in a second memory and to detect an underflow condition. Claim 10 is further amended to clarify that a write address of a third memory is compared with a read address of the third memory to determine whether output data of the second memory are stored in the second memory and to detect an overflow condition, and that data stored in the third memory is output through a single output terminal of the third memory as a display signal for displaying on the display device.

Han discloses a method and apparatus, wherein video data is processed having different formats, such as NTSC and VGA signals (see Han, Figures 3-4 and column 1, lines 6-9). In Han, a pretreater 10 receives a first video having a first format (for example, NTSC) and a second

video having a second format (for example, VGA), converts the second video format into the first video format, and outputs the pretreated video data to a selector 30 (see Han, Figure 4, column 2, lines 45-52 and column 3, lines 6-10). In addition, the pretreater 10 outputs the pretreated video data to a PIP scaler 20 (see Han, Figure 4, column 3, lines 11-13). The selector 30 outputs either the scaled video received from the PIP scaler 20 or the original video data received directly from the pretreater 10 to a series-parallel converter 50 (see Han, Figure 4 and column 3, lines 13-23). A first buffer 60 stores the video data received from the series-parallel converter 50, and the video data is stored in a memory 70 (see Han, Figure 4 and column 4, lines 24-30). A second buffer 100 and a third buffer 110 store the video data read from the memory 70, according to the display format (see Han, Figure 4 and column 3 lines 30-34). A format converter 130 converts the video data received from the second buffer 100 into a data format consistent to a main screen display, and a PIP converter 140 changes the size of the video data received from the third buffer 110 to fit the size of a PIP window (see Han, Figure 4, column 3, lines 34-40). In this manner, a PIP multiplexer 150 selects and displays either the main screen video from the format converter 130 or the PIP video data from the PIP converter 140 (see Han, Figure 4 and column 3, lines 40-44).

It is submitted that Han fails to teach or suggest a first memory for multiplexing second data according to time sharing, storing second data in different regions, and outputting the stored second data in response to a first memory enabling signal, as claimed in amended independent claim 1. Han discloses a first buffer 60 (see Han, Figure 4). However, there is no mention in Han of the first buffer 60 of Han multiplexing second data according to time sharing, as claimed. Further, there is no mention in Han of the first buffer 60 of Han outputting stored second data in response to a first memory enabling signal, as claimed, since, for reasons described below, Han does not teach or suggest the Applicant's claimed first memory enabling signal. It therefore follows that the first buffer 60 of Han is not the first memory, as claimed.

In addition, with regard to claim 1, it is submitted that Han fails to teach a memory control unit for detecting underflow conditions in a first memory, and for generating a first memory enabling signal that is applied to the first memory to control data flow between the first

memory and a second memory, as claimed in amended independent claim 1. Instead, Han discloses a write address generator 90 that generates an address to write the video data from the first buffer 60 to the memory 70 (see Han, Figure 4 and column 3, lines 28-30). However, there is no mention in Han of the write address generator 90 of Han detecting underflow conditions in a first memory, as claimed. Nor is there any mention in Han of the write address generator 90 generating a first memory enabling signal that is applied to a first memory, as claimed. In particular, the write address generator 90 does not generate a first memory enabling signal that is applied to the first buffer 60 to control data flow between the first buffer 60 and the memory 70. It therefore follows that the write generator 90 of Han is not the memory control unit, as claimed.

In addition, with regard to claim 1, it is submitted that Han fails to teach or suggest a memory control unit for generating a frame buffer control signal that is applied to a second memory to control frame rates of input data and to control frame rates of a display signal in response to underflow and overflow conditions, as claimed in claim 1. Instead, Han discloses a read address generator 120 that generates a read address to the memory 70 and outputs data to second and third buffers 100, 110 when amounts of data in second and third buffers 100, 110 fall below a threshold level (see Han, Figure 4 and column 5, lines 21-25). However, there is no mention in Han that the read address generated by the read address generator 120 is a frame buffer control signal that is applied to a second memory to control frame rates of input data and to control frame rates of a display signal in response to underflow conditions of the first memory and overflow conditions of the third memory, as claimed. For at least these reasons, it follows that the read address generator 120 of Han is not the memory control unit, as claimed.

In addition, with regard to claim 1, it is submitted that Han fails to teach or suggest a memory control unit for detecting overflow conditions in a third memory, and for generating a second memory enabling signal that is applied to a third memory to control data flow between a second memory and the third memory, as claimed. While Han teaches that video data is outputted from memory 70 to second and third buffers 100, 110 via memory interface 80 (see Han, Figure 4), there is no mention in Han of a second memory enabling signal being applied to the second and third buffers 100, 110 of Han to control data flow between a second memory

(referred to in the Office Action at page 3 as being met by memory 70 of Han) and a third memory (referred to in the Office Action at page 3 as being met by the second and third buffers 100, 110).

In addition, with regard to claim 1, it is submitted that Han fails to teach or suggest a third memory for storing data output from a second memory and comprising a single output terminal for outputting the stored data as a display signal in response to a second memory enabling signal, as claimed in claim 1. Instead, Han teaches the two abovementioned memories: second buffer 100 and third buffer 110, each receiving video data from the memory interface 80, the video data outputted to the second buffer 100 or third buffer 110 according to the display format (see Han, Figure 4 and column 3, lines 32-34). The second buffer 100 has an output for outputting video data to a format converter 130, wherein the video data is converted into a data format consistent to a main screen display. The third buffer 110 also has an output for outputting video data to a PIP converter 140, wherein the PIP converter 140 changes the size of the video data received from the third buffer 110 to fit the size of a PIP window (see Han, Figure 4, column 3, lines 34-40). Since the second buffer 100 and third buffer 110 outputs video data to the format converter 130 and PIP converter 140, respectively, it follows that the second buffer 100 and third buffer 110 are not the third memory comprising a single output terminal, as claimed in claim 1. Further, there is no mention in Han of the second buffer 100 and third buffer 110 of Han outputting stored data as a display signal in response to a second memory enabling signal, as claimed. For at least these reasons, the second and third buffers 100, 110 of Han are not the third memory, as claimed.

With regard to Suen, *et al.*, Suen, *et al.* discloses a circuit that converts a selected portion of graphics data generated for a computer display into video data for presentation on a selected portion of a television display (see Suen, Figure 1 and column 2, lines 34-37). However, it is submitted that Suen, *et al.* fails to teach or suggest the present invention, as claimed in amended independent claim 1. Suen, *et al.*, like Han, fails to teach or a first memory for multiplexing second data according to time sharing, storing the stored data in different regions, and outputting the stored data in response to a first memory enabling signal, as claimed in amended independent

claim 1. There is no teaching or suggestion in Suen, *et al.* of a first memory, as claimed.

In addition, it is submitted that Suen, *et al.*, like Han, fails to teach or suggest a memory control unit for detecting underflow conditions in a first memory, and for generating a first memory enabling signal that is applied to the first memory to control data flow between the first memory and a second memory, as claimed in claim 1. For at least the reasons described above, Suen, *et al.* fails to teach or suggest a first memory, as claimed. Thus, it follows that Suen, *et al.* fails to teach or suggest a memory control unit for detecting underflow conditions in a first memory, as claimed. It further follows that Suen, *et al.* fails to teach or suggest a memory control unit for generating a first memory enabling signal that is applied to the first memory to control data flow between the first memory and a second memory, as claimed in claim 1.

In addition, it is submitted that Suen, *et al.*, like Han, fails to teach or suggest a memory control unit for generating a frame buffer control signal that is applied to a second memory to control frame rates of input data and to control frame rates of a display signal in response to underflow and overflow conditions, as claimed in claim 1. Specifically, there is no such teaching or suggestion in Suen, *et al.* of a frame buffer control signal being generated by a memory control unit, as claimed.

In addition, it is submitted that Suen, *et al.*, like Han, fails to teach or suggest a memory control unit for detecting overflow conditions in a third memory, and for generating a second memory enabling signal that is applied to a third memory to control data flow between a second memory and the third memory, as claimed. In particular, there is no such teaching or suggestion in Suen, *et al.* of a second memory enabling signal being generated by a memory control unit, as claimed.

In addition, it is submitted that Suen, *et al.*, like Han, fails to teach or suggest a third memory for storing data output from a second memory and comprising a single output terminal for outputting the stored data as a display signal in response to a second memory enabling signal, as claimed. In particular, there is no teaching or suggestion in Suen, *et al.* of a third memory comprising a single output terminal for outputting stored data as a display signal in response to a second memory enabling signal, as claimed.

With regard to claim 10, it is submitted that the combination of Han nor Suen, *et al.* fails to teach or suggest comparing a write address of a first memory with a read address of the first memory to determine whether data stored in the first memory are stored in a second memory and to detect underflow conditions in the first memory, as claimed in amended independent claim 10. Neither reference teaches or suggests a first memory, as claimed, for at least the reasons described above. With regard to Han, while Han teaches a write address generator 90 that generates an address to write the video data from the first buffer 60 to the memory 70, and Han further teaches a read address generator 120 that generates a read address to the memory 70 and outputs data to second and third buffers 100, 110 when amounts of data in second and third buffers 100, 110 fall below a threshold level, there is no mention in Han of the write address of a first memory of Han being compared with the read address of a first memory of Han, as claimed in claim 10.

In addition, with regard to claim 10, it is submitted that the combination of Han nor Suen, *et al.* fails to teach or suggest comparing a write address of a third memory with a read address of the third memory to determine whether output data of the second memory are stored in the second memory and to detect overflow conditions in the third memory, and outputting data stored in the third memory through a single output terminal of the third memory as a display signal for displaying on the display device, as claimed in amended independent claim 10. Neither reference teaches or suggests a single output terminal of a third memory, as claimed, for at least the reasons described above. Therefore, neither reference teaches or suggests a third memory, as claimed. It therefore follows that neither reference teaches or suggests comparing a write address of a third memory with a read address of the third memory, as claimed in claim 10.

It is therefore submitted that neither Han nor Suen, *et al.* teaches or suggests elements of the claims set forth above. Specifically, neither reference teaches or suggests a first memory for multiplexing second data according to time sharing, storing the stored data in different regions, and outputting the stored data in response to a first memory enabling signal, as claimed in amended independent claim 1. In addition, neither reference teaches or suggests a memory control unit for (i) detecting underflow conditions in a first memory and detecting overflow

conditions in a third memory, (ii) generating a first memory enabling signal that is applied to the first memory to control data flow between the first memory and a second memory, (iii) generating a frame buffer control signal that is applied to the second memory to control frame rates of the input data and to control frame rates of the display signal in response to the underflow and overflow conditions, and (iv) generating the second memory enabling signal that is applied to the third memory to control data flow between the second memory and the third memory, as claimed in amended independent claim 1. In addition, neither reference teaches or suggests a third memory for storing data output from a second memory and comprising a single output terminal for outputting the stored data as a display signal in response to a second memory enabling signal, as claimed in claim 1. In addition, neither reference teaches or suggests comparing a write address of a first memory with a read address of the first memory to determine whether data stored in the first memory are stored in a second memory and to detect underflow conditions in the first memory, as claimed in amended independent claim 10. In addition, neither reference teaches or suggests comparing a write address of a third memory with a read address of the third memory to determine whether output data of the second memory are stored in the second memory and to detect overflow conditions in the third memory, and outputting data stored in the third memory through a single output terminal of the third memory as a display signal for displaying on the display device, as claimed in claim 10.

Since neither Han nor Suen, *et al.* teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set forth in the amended claims.

Since Han and Suen, *et al.*, taken alone or in combination, fail to teach or suggest the present invention set forth in the amended claims, claims 1, 10, 12, and 20 are believed to be allowable over the cited references. Accordingly, reconsideration of the rejections of claims 1, 10, 12, and 20 under 35 U.S.C. 103(a) based on Han and Suen, *et al.* is respectfully requested.

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such

allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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